What is claimed is:

1. A semiconductor chip package comprising:

an interconnection substrate;

a peripheral substrate having an opening;

a central substrate being disposed in the opening of the peripheral substrate and substantially coplanar with the peripheral substrate, wherein the central substrate and the peripheral substrate are mechanically and electrically connected to the interconnection substrate;

a semiconductor chip sandwiched between the interconnection substrate and the central substrate, the interconnection substrate having a recessed cavity for receiving the semiconductor chip;

a plurality of central solder balls disposed on a bottom surface of the central substrate and electrically connected to the semiconductor chip; and

a plurality of peripheral solder balls disposed on a bottom surface of the peripheral substrate and electrically connected to the semiconductor chip through the interconnection substrate,

wherein the peripheral substrate is substantially separated from the central substrate thereby decreasing the stresses on the peripheral substrate due to coefficient of thermal expansion mismatch.

2. The semiconductor chip package as claimed in claim 1, wherein

the interconnection substrate has a bottom surface provided with a plurality of contact pads around the recessed cavity;

the central substrate has a top surface provided with a plurality of first and second contact pads, wherein the second contact pads are electrically connected to the first contact pads;

the peripheral substrate has a top surface provided with a plurality of contact pads;

the semiconductor chip is provided with a plurality of bonding pads and disposed on the top surface of the central substrate by flip-chip bonding such that the bonding pads of the semiconductor chip are electrically connected to the first contact pads of the central substrate;

the central solder balls are electrically connected to the bonding pads of the semiconductor chip through the first contact pads of the central substrate; and

the peripheral solder balls are electrically connected to the semiconductor chip through the contact pads of the peripheral substrate and the second contact pads of the central substrate.

3. The semiconductor chip package as claimed in claim 1, wherein the interconnection substrate comprises a top plate and a dielectric layer securely attached to the top plate, and the dielectric layer has an opening integrated with the top plate to form the recessed cavity of the interconnection substrate.

4. The semiconductor chip package as claimed in claim 3, wherein the top plate of the interconnection substrate comprises a heat-sink.

5. The semiconductor chip package as claimed in claim 1, further comprising a metal plate sandwiched between the semiconductor chip and the interconnection substrate.

6. The semiconductor chip package as claimed in claim 1, wherein the central substrate and the peripheral substrate are mechanically and electrically connected to the interconnection substrate by a plurality of solder balls.

7. The semiconductor chip package as claimed in claim 1, wherein the central substrate and the peripheral substrate are completely separated from each other.

8. The semiconductor chip package as claimed in claim 1, wherein the central substrate and the peripheral substrate are separated by a plurality of slots and partially connected to each other.

9. A method for manufacturing a semiconductor chip package, the method comprising the following steps of:

mechanically and electrically connecting a semiconductor chip to a top surface of a main substrate;

securely attaching the semiconductor chip to a recessed cavity on a bottom surface of an interconnection substrate;

mechanically and electrically connecting the main substrate with the semiconductor chip to the interconnection substrate;

cutting the main substrate to form a central substrate and a peripheral substrate substantially separated from each other, wherein the semiconductor chip is disposed on the central substrate.

10. The method as claimed in claim 9, further comprising the step of attaching a dielectric layer with an opening to a top plate thereby forming the interconnection substrate having the recessed cavity.

11. The method as claimed in claim 10, wherein the top plate of the interconnection substrate comprises a heat-sink.

12. The method as claimed in claim 9, further comprising the step of disposing a metal plate between the semiconductor chip and the interconnection substrate.

13. The method as claimed in claim 9, wherein semiconductor chip is connected to the main substrate by flip-chip bonding.

14. The method as claimed in claim 9, further comprising the step of forming a plurality of solder balls on contact pads around the recessed cavity on the bottom surface of the interconnection substrate before the step of connecting the main substrate to the interconnection substrate, wherein the step of connecting the main substrate to the interconnection substrate comprises a step of reflowing the solder balls.

15. The method as claimed in claim 9, further comprising the step of forming a plurality of solder balls on a bottom surface of the main substrate before the step of cutting the main substrate.

16. The method as claimed in claim 9, further comprising the step of forming a plurality of solder balls on a bottom surface of the main substrate after the step of connecting the semiconductor chip to the main substrate and before the step of attaching the semiconductor chip to the interconnection substrate.

17. The method as claimed in claim 9, wherein the central substrate from the peripheral substrate is completely separated from each other after the cutting step is conducted.

18. The method as claimed in claim 9, wherein the cutting step is conducted by forming a plurality of slots such that the central substrate and the peripheral substrate is partially connected to each other.

19. A substrate for use in a semiconductor chip package, the substrate comprising:

opposing top and bottom surfaces;

a plurality of chip bonding pads disposed on the top surface of the substrate adapted for electrically connecting to a semiconductor chip;

a plurality of central contact pads disposed on the bottom surface of the substrate and electrically connected to the chip bonding pads;

a plurality of peripheral contact pads disposed on the bottom surface of the substrate; and

a plurality of slots disposed between the central contact pads and the peripheral contact pads for separating the central contact pads and the peripheral contact pads.

20. A semiconductor chip package comprising:

a main substrate comprising a plurality of chip bonding pads disposed on a top surface of the main substrate, a plurality of central contact pads and a plurality of peripheral contact pads disposed on a bottom surface of the main substrate and electrically connected to the chip bonding pads, and a plurality of slots disposed between the central contact pads and the peripheral contact pads for separating the central contact pads and the peripheral contact pads; and

a semiconductor chip disposed on the upper surface of the main substrate and electrically connected to the chip bonding pads.

21. The semiconductor chip package as claimed in claim 20, further comprising an interconnection substrate wherein the main substrate is mechanically and electrically connected to the interconnection substrate, and the semiconductor chip is sandwiched between the interconnection substrate and the main substrate.

22. The semiconductor chip package as claimed in claim 21, wherein the interconnection substrate has a recessed cavity for receiving the semiconductor chip.

23. The semiconductor chip package as claimed in claim 22, wherein the interconnection substrate comprises a top plate and a dielectric layer securely attached to the top plate, and the dielectric layer has an opening integrated with the top plate to form the recessed cavity of the interconnection substrate.

24. The semiconductor chip package as claimed in claim 23, wherein the top plate of the interconnection substrate comprises a heat-sink.

25. The semiconductor chip package as claimed in claim 21, further comprising a metal plate sandwiched between the semiconductor chip and the interconnection substrate.

26. The semiconductor chip package as claimed in claim 21, wherein the main substrate is mechanically and electrically connected to the interconnection substrate by a plurality of solder balls.

27. The semiconductor chip package as claimed in claim 20, further comprising a plurality of contact pads provided on the top surface of the main substrate.